REMARKS/ARGUMENTS

In response to the above-identified Office Action, Applicant has amended claims 1, 11, 13, and 17. Claims 1-17 remain pending in the present application.

For the reasons set forth more fully below, Applicant respectfully submits that the present claims are allowable. Consequently, reconsideration, allowance and passage to issue of the present application are respectfully requested.

Applicant has amended the specification to update co-pending application references. Applicant respectfully submits that no new matter has been added.

Applicant has amended independent claims 1 and 13 to include the recitation of 'each instruction code,' rather than 'an instruction code,' as originally recited in independent claim 7. Applicant also has amended claims 11 and 17 to correct minor typographical errors in these claims. Applicant respectfully submits that no new matter has been added nor has the scope of the claims been changed by these amendments.

Cited Art Rejection

The Examiner rejected claims 1-17 under 35 U.S.C. 102(a) as being anticipated by Ebicioglu et al ("Ebicioglu"). Applicant respectfully disagrees with the rejection.

The present invention provides a method and system for encoding instructions as a very long instruction word (VLIW) for processing in a plurality of computation units that reduces instruction memory requirements in a processing system. The present invention determines at which stages of instruction processing that each instruction code of the very long instruction word needs to be executed. Further, an enable signal of the instruction code is utilized to direct execution during the determined stages by enabling storage operations for each instruction code. See independent claims 1 and 13. The present invention also recites encoding each instruction code of the very long instruction word as an enable signal and an action signal to collapse instruction fields in the very long instruction word, and associating each instruction code with a

computation unit. See independent claim 7. Through the present invention, less memory is required to store instructions.

In the rejection, the Examiner asserts that Ebicioglu discloses a VLIW system that determines at which stages that an instruction needs or should be executed and uses an enable signal of the instruction in the form of condition codes to direct execution by enabling storage operation. Applicant respectfully submits that Ebicioglu fails to teach, show, or suggest the recited invention.

Ebicioglu is concerned with how to execute a computer program, complied for sequential execution, on a parallel instruction processing system. The condition codes (cc) of Table 3 pointed by the Examiner in the cited section of column 10 of Ebicioglu provide an indicator of a value needed in order to take a particular branch in the computer program. The cc values are based on a branch operation and branch condition of the branch instruction. Thus, these values are used solely for branch instructions existing in the sequential instructions. They are not taught or suggested as being present for each instruction in the VLIW. Similarly, the bit masks of Table 4 pointed to by the Examiner in the cited section of column 10 are not taught or suggested for use with each instruction in the VLIW. Rather, they are branching indicators for those integer operations that are part of a branch of the sequential instructions. Applicant further respectfully submits that Ebicioglu teaches that the flagging of integer instructions in the form of fixed- and floating-point instructions occurs only when those instructions are inserted after a conditional branch to indicate their branch dependency (col. 4, lines 28-31). Applicant fails to see how these disparate condition codes and bit masks/flags used for selected instructions teach, show, or suggest an enable signal encoded in each instruction code in a VLIW, or further, an enable signal encoded in each instruction code that directs execution by enabling storage operations for each instruction code, as recited by the Applicant in varying form in independent claims 1, 7, and 13.

Accordingly, Applicant respectfully submits that the cited art of Ebicioglu fails to teach, show, or suggest the recited invention of independent claims 1, 7, and 13. Further, claims 2-6, 8-

12, and 14-17 depend directly or indirectly on an independent claim, and therefore, are respectfully submitted as allowable for at least those reasons presented hereinabove.

In view of the foregoing, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. 102(a).

Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

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Date

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